AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Original) A speed binning test circuit, comprising:

a plurality of circuit groups arranged along a boundary of a chip circuit, each circuit group including a different number of unit delay circuits; and

a plurality of pads, each pad arranged so that at least one output terminal of unit delay circuits of the plurality of circuit groups is connected to each of the pads, respectively.

2. (Original) The speed binning test circuit of claim 1, wherein the plurality of circuit groups include:

a first speed correlation circuit in which unit delay circuits of a first group are serially-connected to one another for delaying a received final delay signal and outputting a first delay signal;

a second speed correlation circuit in which unit delay circuits of a second group are serially-connected to one another for delaying the first delay signal and outputting a second delay signal;

a third speed correlation circuit in which unit delay circuits of a third group are serially-connected to one another for delaying the second delay signal and outputting a third delay signal; and

a fourth speed correlation circuit in which unit delay circuits of a fourth group are serially-connected to one another for delaying the third delay signal and outputting the final delay signal that is received by the first group of unit delay circuits.

3. (Original) The speed binning test circuit of claim 1,

wherein the ratio of numbers of unit delay circuits of the plurality of circuit groups are expressed by:

$$A:B:C:D = a:b:c:d,$$

wherein A denotes a number obtained by subtracting 1 from the numbers of unit delay circuits of a first group; B denotes the number of unit delay circuits of a second group; C denotes the number of unit delay circuits of a third group; D denotes a number of unit delay circuits of the fourth group, and

wherein a, b, c, and d represent different valued coefficients.

4. (Original) The speed binning test circuit of claim 3, wherein a, b, c, and d are different prime numbers.

5. (Original) The speed binning test circuit of claim 2, wherein the first through third delay signals, collectively, and the final delay signal have the same oscillation waveforms after a given time.

6. (Original) The speed binning test circuit of claim 5, wherein the given time represents a total signal delay time of a signal delayed through the first through fourth groups.

7. (Original) The speed binning test circuit of claim 1, wherein the unit delay circuits are inverter circuits.

8. (Original) A semiconductor device, comprising:

a plurality of signal input/output pins;

a core circuit including logic that receives or outputs a signal via the plurality of signal input/output pins; and

a speed binning test circuit composed of a plurality of circuit groups, each circuit group including a different number of unit delay circuits arranged in a chain structure along the boundary of the core circuit.

9. (Original) The semiconductor device of claim 8, wherein the speed binning test circuit comprises:

a first speed correlation circuit in which unit delay circuits of a first group are serially-connected to one another for delaying a received final delay signal and outputting a first delay signal;

a second speed correlation circuit in which unit delay circuits of a second group are serially-connected to one another for delaying the first delay signal and outputting a second delay signal;

a third speed correlation circuit in which unit delay circuits of a third group are serially-connected to one another for delaying the second delay signal and outputting a third delay signal;

a fourth speed correlation circuit in which unit delay circuits of a fourth group are serially-connected to one another for delaying the third delay signal and outputting the final delay signal that is received by the first group of unit delay circuits; and

a plurality of pads, each pad arranged so that at least one output terminal of unit delay circuits of the plurality of circuit groups is connected to each of the pads, respectively.

10. (Original) The semiconductor device of claim 8,

wherein the ratio of numbers of unit delay circuits of the plurality of circuit groups are expressed by:

$$A:B:C:D = a:b:c:d,$$

wherein A denotes a number obtained by subtracting 1 from the numbers of unit delay circuits of a first group; B denotes the number of unit delay circuits of a second group; C denotes the number of unit delay circuits of a third group; D denotes a number of unit delay circuits of the fourth group, and

wherein a, b, c, and d represent different valued coefficients.

11. (Original) The semiconductor device of claim 10, wherein a, b, c, and d are different prime numbers.

12. (Original) The semiconductor device of claim 9, wherein the first through third delay signals, collectively, and the final delay signal have the same oscillation waveforms after a given time.

13. (Original) The semiconductor device of claim 12, wherein the given time represents a total signal delay time of a signal delayed through the first through fourth groups.

14. (Original) The semiconductor device of claim 8, wherein the unit delay circuits are inverter circuits.

15. (Previously Presented) A speed binning test method, comprising:

delaying test signals through a plurality of successively connected circuit groups, each of the plurality of successively connected circuit groups including different number of unit delay circuits, that forms a chain structure on a chip, and

monitoring on-chip-variations to determine total signal delay time through the chain structure.

16. (Previously presented) The method of claim 15, further comprising receiving the test signals from a core circuit on the chip via a plurality of signal input/output pins.

17. (Canceled)

18. (Original) The method of claim 15, wherein the delaying step further includes:

first delaying a received final delay signal and outputting a first delay signal in a first group of the plurality of successively connected circuit group;

second delaying the first delay signal and outputting a second delay signal in a second group of the plurality of successively connected circuit group;

third delaying the second delay signal and outputting a third delay signal in a third group of the plurality of successively connected circuit group; and

fourth delaying the third delay signal and outputting the final delay signal that is received by the first group in a fourth group of the plurality of successively connected circuit group.

19. (Previously Presented) The method of claim 18, wherein the monitoring step further includes monitoring on-chip variations by measuring oscillation waveforms at a plurality of pads connected to at least one output terminal of unit delay circuit of the circuit groups, respectively that form the chain structure.

20. (Original) The method of claim 19, wherein the first through third delay signals, collectively, and the final delay signal have the same oscillation waveforms after a given time.

21. (Original) The method of claim 20, wherein the given time represents a total signal delay time of a signal delayed through the first through fourth groups.

22. (Original) The method of claim 15,

wherein the ratio of numbers of unit delay circuits of the plurality of circuit groups are expressed by:

$$A:B:C:D = a:b:c:d,$$

wherein A denotes a number obtained by subtracting 1 from the numbers of unit delay circuits of a first group; B denotes the number of unit delay circuits of a second group; C denotes the number of unit delay circuits of a third group; D denotes a number of unit delay circuits of the fourth group, and

wherein a, b, c, and d represent different valued coefficients.

23. (Original) The method of claim 22, wherein a, b, c, and d are different prime numbers.

24. (Canceled)

25. (Canceled)

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